MIPS interAptiv Processor Core

MIPS interAptiv is a family of multi-core, multi-threaded 32-bit processors.

The use of multi-threading, improvements to multi-core performance, and additional core enhancements for error correction and power management make interAptiv among the most performance-efficient and feature-rich CPU cores in its class.

With the MIPS interAptiv CPU, designers have access to two virtual processing elements (VPEs), or hardware threads, which appear as two complete processors to an SMP (symmetric multiprocessing) operating system.

These threads efficiently use a shared execution pipeline resulting in very high efficiency in terms of area and power relative to competing cores in the same class, as measured by the industry-standard CoreMark benchmark. Threads can also be managed using the hardware scheduler and inter-thread communication features. High efficiency and access to thread-level management make the interAptiv CPU the ideal solution for applications that are highly threaded and require support for Quality of Service (QoS).

The MIPS interAptiv CPU utilizes the second generation Coherence Manager (CM2) interconnect, which has an integrated L2 cache. The CM2 improves multi-core performance by simultaneously reducing latency and increasing bandwidth. The CM2 supports up to four interAptiv CPUs or eight virtual processors in a single, fully coherent, multi-processor system.

As an increasing amount of data is stored and transported to and from a variety of embedded client devices and storage infrastructure equipment, data reliability is a growing requirement. The interAptiv CPU, which has Error Correction Code (ECC) support on data memories, makes it a great fit for higher reliability applications such as RAID storage and automotive driver assistance.

The interAptiv CPU, with its robust ability to control power at both the cluster and core levels, makes power management a snap for SoC designers.
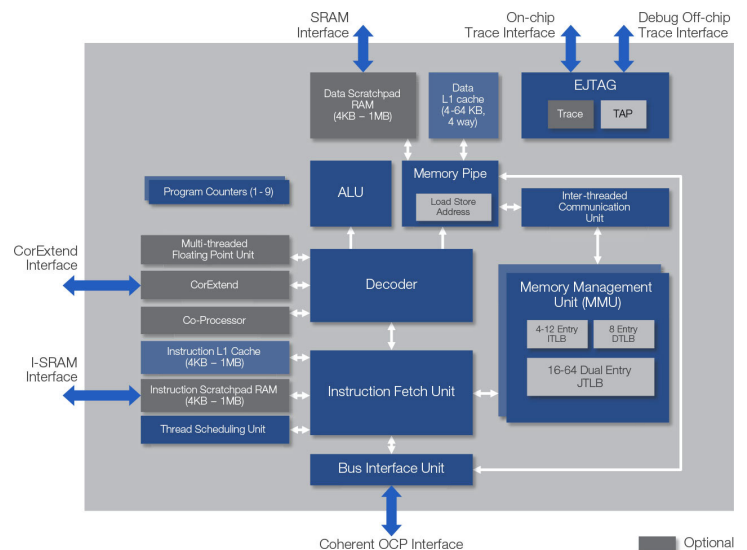
About Wave Computing

Wave Computing, Inc. is revolutionizing AI with its dataflow-based systems and solutions that deliver orders of magnitude performance improvements over legacy architectures. The company's vision is to bring deep learning to customers' data wherever it may be—from the edge to the datacenter—helping accelerate time-to-insight. Wave is powering the next generation of AI by combining its dataflow architecture with its MIPS embedded RISC multithreaded CPU cores and IP. Wave Computing has been named Frost & Sullivan's 2018 "Machine Learning Industry Technology Innovation Leader," and recognized by CIO Application Magazine's as one of the "Top 25 Artificial Intelligence Providers." Combined with MIPS, Wave now has over 400 granted and pending patents and hundreds of customers worldwide.

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